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Investigating Enhancement Mode Gallium Nitride Power FETs in High Voltage, High Frequency Soft Switching Converters

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Keywords: Gallium Nitride, Soft Switching, ZVS Buck.

Abstract

An increased attention has been detected to develop smaller and lighter high voltage power converters in the range of 50V to 400V domain. The main applications for these converters are mainly focused for Power over Ethernet (PoE), LED lighting and AC adapters. This work will discuss a study of using enhancement mode gallium nitride switches to form a 50V quasi-square-wave zero-voltage-switching buck converter running at 2-6 MHz under full load. The designed converter achieved 83% efficiency converting 50V input voltage to 12.2V at 9W load.

1 Introduction

The demand for smaller size and lighter weight power converters has led the development of higher switching frequency converters. With silicon MOSFETs reaching its performance limits [1], new routes for research have led to achieve switching at high frequency (3MHz - 30MHz) and above [2, 3, 4, 5, 6, 7]. These routes are new semiconductor materials, innovative packaging, and converter topologies in addition to high frequency passives development.

Operating at high frequencies enables the integration of the magnetic components and other passive elements achieving higher power densities [8]. For high input voltage converters, operating at high frequency should be combined with a kind of soft switching techniques to avoid excess power losses which can lead to converter thermal run-away. For sake of integrating and increasing the power densities to higher levels, wide bandgap materials provided the needed switching performance.

It has been reported by many researchers that gallium nitride (GaN) devices has promising figure of merits (FOM). The theoretical lateral devices on-resistance of the MOSFET times the gate charge of GaN was reported in Figure.1 which shows the superiority of GaN HEMT for two different feature sizes especially at higher breakdown voltages [9].

This paper investigates the advantages and requirements of using enhancement mode gallium nitride (eGaN) based switches in a high frequency high voltage power converter.

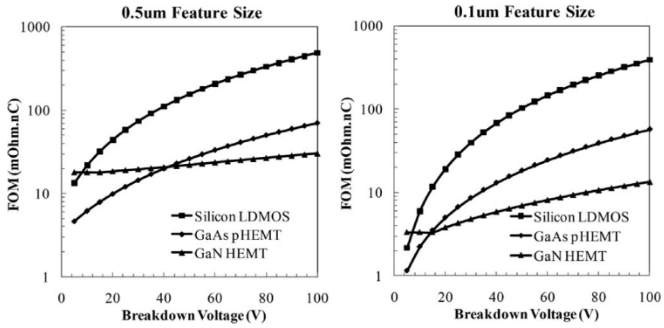


Figure 1: Analytical FOM of lateral power switches: Si NMOS, GaAs pHEMT, and GaN HEMT for two minimum feature sizes [9]

2 Gallium Nitride Versus Silicon

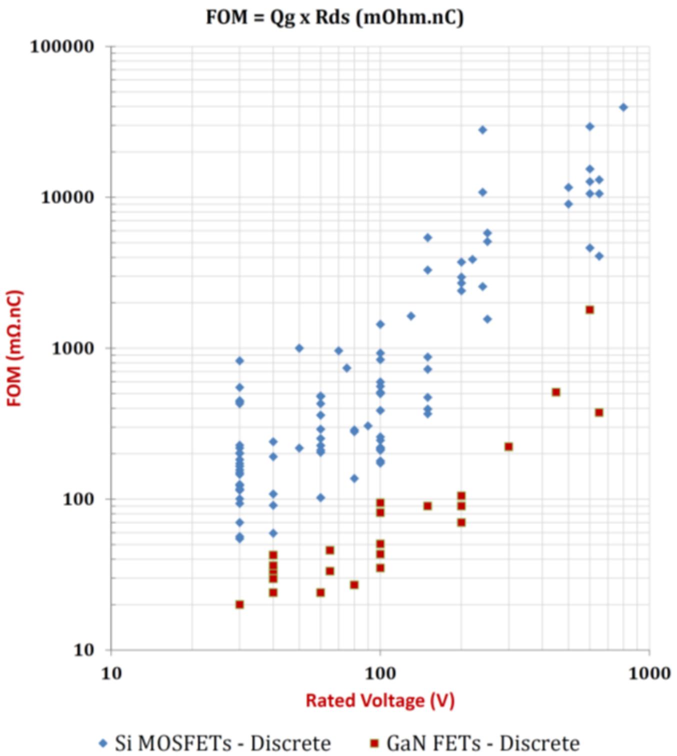
Gallium nitride has a higher bandgap and electron mobility compared to silicon, silicon carbide and gallium arsenide which make gallium nitride the preferred material for this research [3]. GaN FETs have a potential for development. It is more expensive than silicon counterparts but with designs shift towards using them will reduce the price and hopefully enables more integration into the same die. The authors collected FETs parameters to compart the figure of merits for silicon switches and GaN switches. The results were collected from more than 140 MOSFET datasheets.

The first figure of merit represents the on-resistance of the switch times the total gate charge is shown in figure 2a. The resulting graph shows the superiority of GaN devices over silicon devices and the gap increases as high as the breakdown voltage goes.

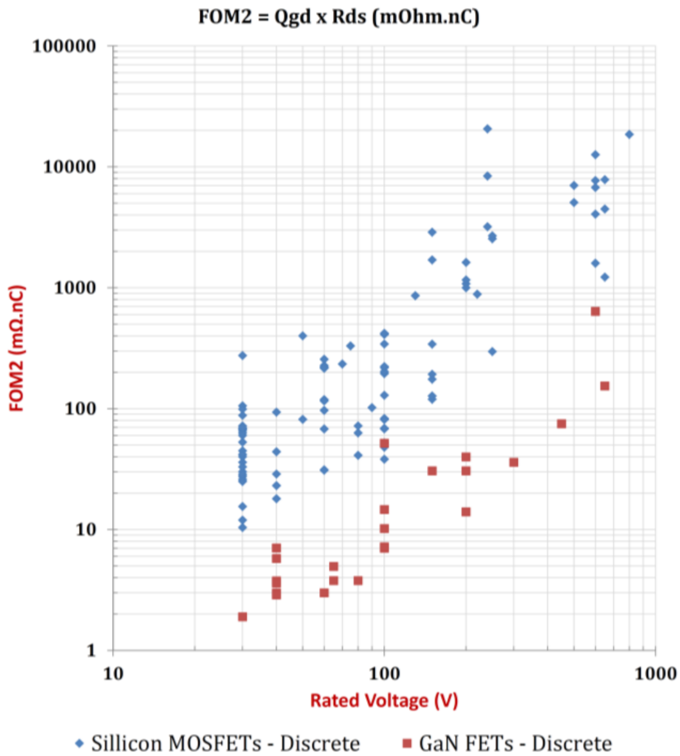
Figure 2b shows a second figure of merits graphed against maximum drain to source voltage. The second FOM represents the gate to drain charge times the on-resistance of the switch. The figure also shows better GaN performance compared to silicon.

3 Theory of QSW-ZVS Buck Converter

The most basic step down switching converter is the buck converter. The buck converter can operate in a continuous-



a. summary of high voltage FETs $Q_{gtot}.R_{ON}$



b. summary of high voltage FETs $Q_{gd}.R_{ON}$

Figure 2: Summary of gallium nitride FETs vs. silicon MOSFETs figure of merits

conduction mode (CCM) or in a discontinuous conduction mode (DCM), depending on the waveform of the inductor current. In CCM, the inductor current flows during the entire cycle, whereas in DCM the inductor current flows only during part of the cycle. In DCM, it falls to zero and remains at zero for some time interval, before it starts to rise again in the next cycle. Operation at the boundary between CCM and DCM is called the critical conduction mode as shown in figure.3. For synchronous buck converter, which uses two switches to chop the input DC voltage, the inductor current will be continuous even if it falls under zero as a result of using bidirectional switches [10].

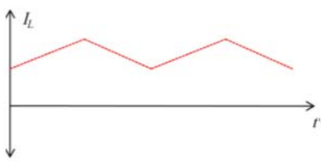
Zero-Voltage-Switching Quasi-Square-Wave (ZVS-QSW) is a switching technique which uses the current passing through a switch to charge or discharge the output capacitance of a semiconductor switch resulting in much lower output capacitance related switching losses [2, 7]. ZVS technique is based on turning-on the power MOSFET switches when the drain to source voltage drops to zero volt (i.e. V_{DS} = 0) to mitigate the switching and diode reverse recovery losses. ZVS-QSW is the simplest technique used to achieve soft switching by simply reducing the output inductance L_O under the critical value and using bi-directional switches to avoid main current discontinuity. QSW-ZVS buck converter can be realized by designing the inductor value to be less than the inductor value needed to operate a buck converter in critical conduction mode which is given by Equation.1 [10].

$$\mathrm{L_{O(min)}} = \frac{(1-\mathrm{D})}{2\mathrm{F_{SW}}}\mathrm{R_{Load}} \qquad (1)$$

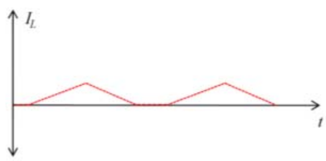
For QSW-ZVS operation, it is important to assure the inductor current has the needed negative valley value based on equation.2 [10].

$$\mathrm{I_{Lo\,(min)}} = \mathrm{I_{Load}} - \frac{\Delta \mathrm{I_{Lo}}}{2} = \frac{\mathrm{V_O}}{\mathrm{R_{Load}}} - \frac{\mathrm{V_O}}{2\mathrm{L_O F_{SW}}}(1-\mathrm{D}) \qquad (2)$$

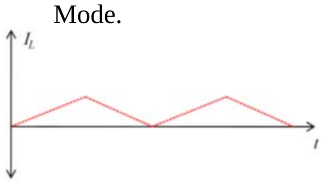
Accurate gate drive timing is needed to achieve zero voltage switching and also to reduce the power loss in body diodes or power loss due to reverse conduction charge [10, 11]. Simple QSW-ZVS buck converter and ideal waveforms are shown in Figure.4.



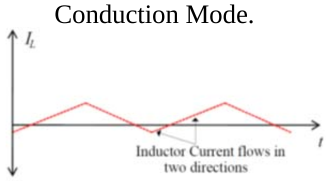
(a) Continuous Conduction Mode.



(b) Discontinuous Conduction Mode.

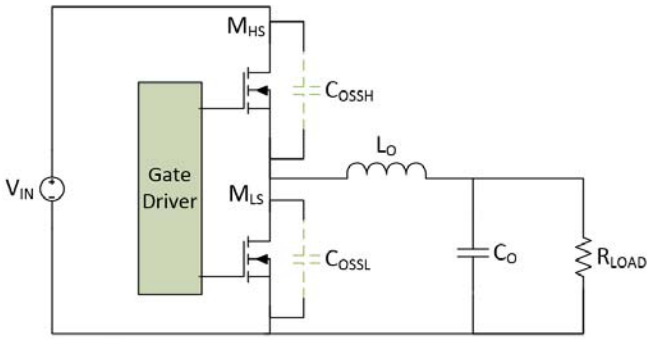


(c) Critical Conduction Mode.

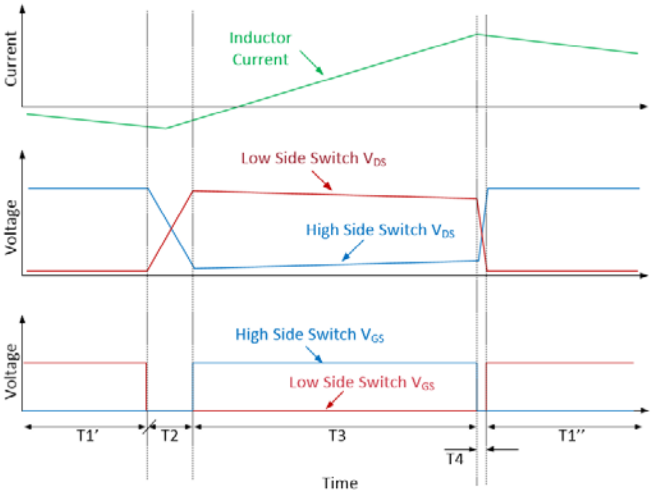


(d) Continuous Conduction Mode Using Bidirectional Switches.

Figure 3: Basic Buck Converter Modes of Operation [10].



(a) Power stage schematic.



(b) Converter waveforms at heavy load.

Figure 4: Simple QSW-ZVS Buck Converter

To understand how QSW-ZVS buck converter works in steady state, the switching period -which is shown in figure 4b- was divided into four sub-periods [11].

a. Sub-Period 1 [T1' and T1"]:
   In this sub-period, the low side switch is fully ON and the high side switch is OFF. The switching node voltage equals the voltage drop across the low side switch. The inductor current is decreasing less than zero at this period.
b. Sub-Period 2 [T2]:
   This sub-period starts when the duty cycle signal forces the low side switch to turn off. The voltage across the low side switch starts to rise due to the negative inductor current is charging its output capacitance and the voltage across the higher side switch is falling to zero. When the voltage across the high side switch reaches zero, the high side driver turns the high side switch on.
c. Sub-Period 3 [T3]:
   In this sub-period, the low side switch is OFF and the upper side switch is ON. The switching node voltage is equal to the voltage drop across the high side switch subtracted from the input Voltage. The inductor current is rising to its maximum value at the end of duty cycle.
d. Sub-Period 4 [T4]:
   This sub-period starts from the end of duty cycle input signal. The driver forces the high side switch to switch off. The positive direction inductor current quickly discharge the capacitances connected to the switching node. The voltage of the switch node drops to zero. When the voltage across the low side switch reaches zero, the low side driver forces the switch to be "ON".

In case of operating a ZVS-QSW converter in light load the inductor average current should be equal to the load current, and the peak and the valley of inductor current will be changed. Consequently, the slew rate of switching node will be changed based on the load current. The optimum gate signal timing should be modified to avoid shoot-through problems if short dead-time is provided and avoiding body diode losses if large dead-time is provided. If the gate signalling is not optimized, it will lead to lower obtained efficiencies.

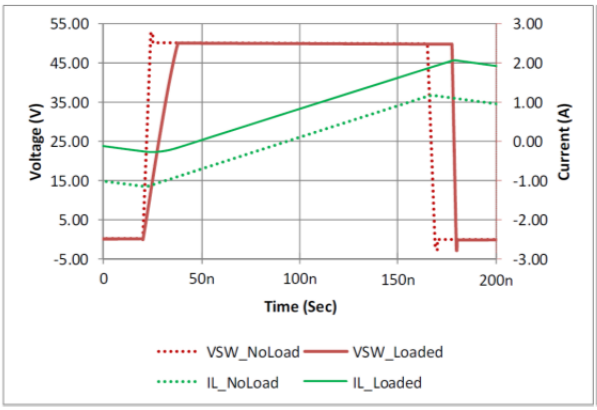
4 System Description and Simulation Results

A QSW-ZVS converter was built using 100V eGaN FETs but the input voltage was limited to 50V for this experiment. Two variants of the converter were tested at two different frequencies for investigation. With a change in the inductor and the switching frequency, a converter running at 2MHz uses a 2.2uH inductor and a 6MHz converter with 500nH air core inductor.
The two converters were simulated using a SPICE based simulation tool. Figure 5 shows the converter simulation results running at 2MHz. The inductor current and the switching node voltage have been shown the first subplot. The gate signals at no load condition have been shown in the second subplot. The third subplot shows the gate signal at full load.
It is obvious from the simulation results that the rise time and the fall time of the switching node voltage is load dependant.
The gate signalling is changed manually to give the best results.

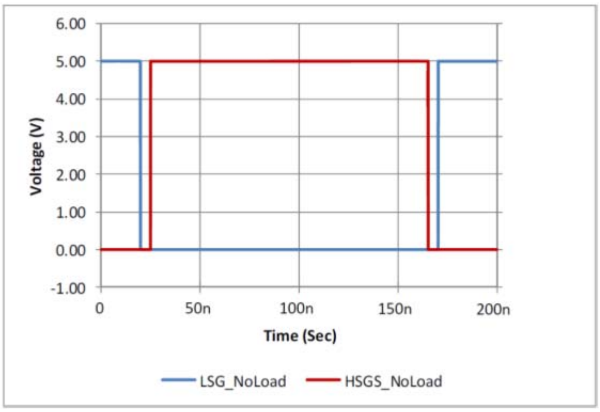
5 Experimental Setup and Results

A printed circuit board was assembled to form the power stage. The inputs for the gate driver were provided through a signal generator connected to two BNC connectors on the test board shown in figure 6. The signal generator is used to fine tune the dead time to achieve zero voltage switching.
The first converter was assembled and tested at 2MHz and using a 2.2uH inductor. Switching node and the inverse duty cycle waveforms are shown in figure 7 where the first sub-graph shows the no-load waveforms. The waveforms show some reverse conduction due to the inserted dead-time. Figure 7.b shows the waveforms at full load of 9 watts at 13.2V output voltage. The switching node waveform shows the obvious low dv/dt for the switching voltage rise time at full load.

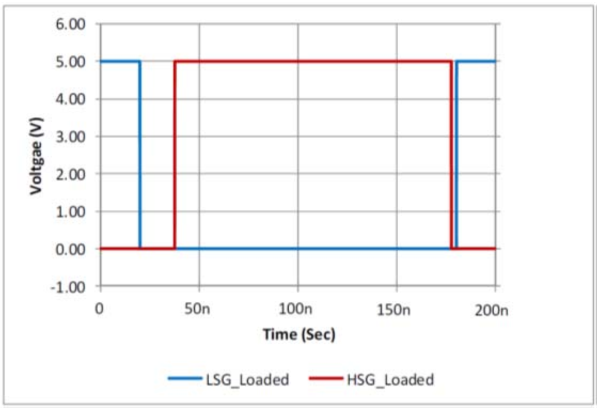
The second converter was built to switch at 6MHz and the inductor was changed to 500nH air core inductor as shown in figure 8. Figures 8.a and 8.b show the converter switching node and the inverse duty cycle of the converter running at 6MHz at no load and full load respectively.
The converter switching at 6MHz achieved 83% efficiency at full load. On the other hand the converter which is running at 2MHz achieved 75% efficiency at full load it was noted that the inductor dominated the power losses.



(a) Switching node voltage and inductor current under full load and no load conditions



(b) Gate to source voltage for high side and low side FETs at no load



(c) Gate to source voltage for high side and low side FETs at full load

Figure 5: Simulation Results of the GaN converter switching at 2 MHz

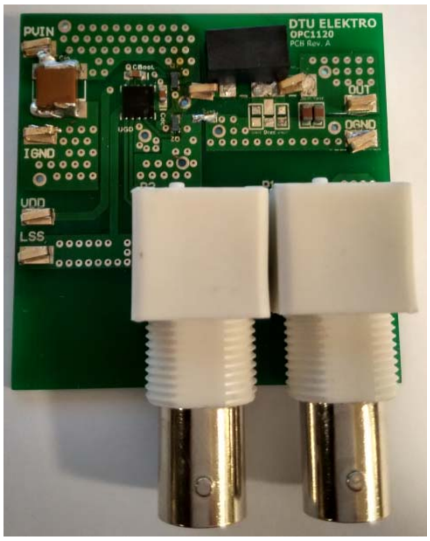
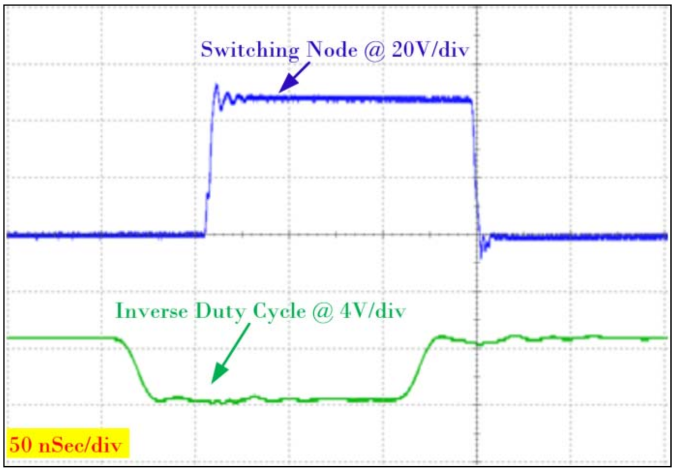
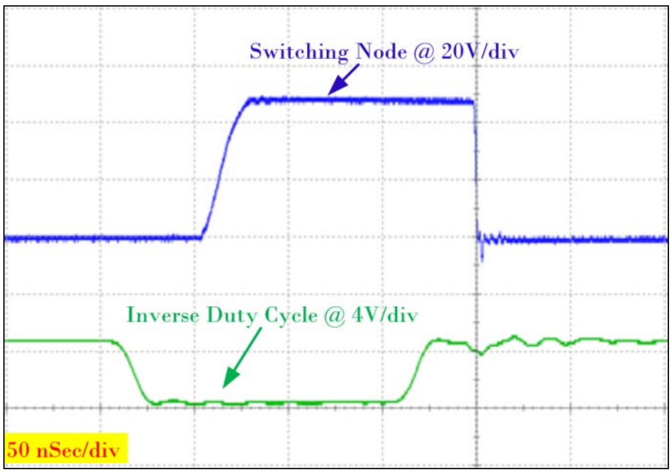


Figure 6: a Photograph of the test PCB

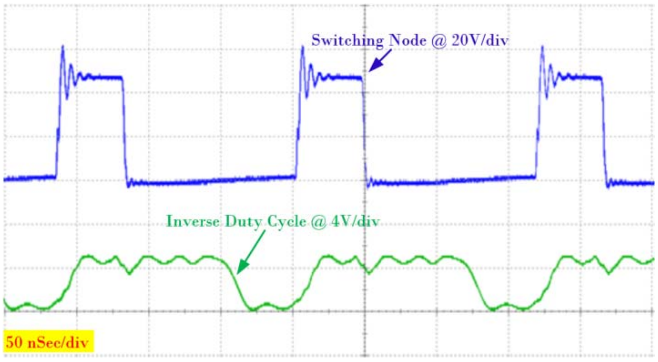


(a) No Load Condition

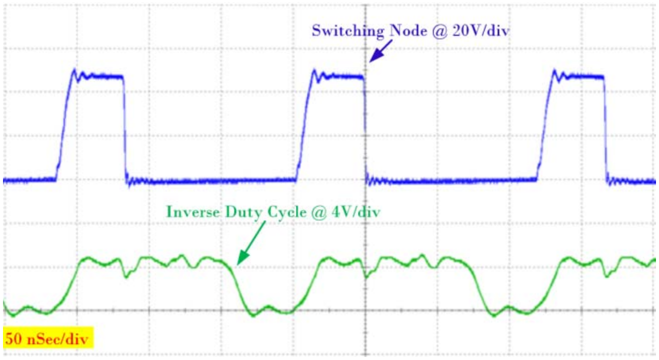


(b) Full Load Condition

Figure 7: Experimental waveforms of switching node and inverse duty cycle at 2 MHz



(a) No Load Condition



(b) Full Load Condition

Figure 8: Experimental waveforms of switching node and inverse duty cycle at 6MHz

6 Conclusion

In this study, gallium nitride devices show promising results. Gate driver and dead time should be accurately fine-tuned on-the-fly not only to achieve high efficiencies but also to prevent hard switching from happening and causing a damage to the converter. QSW-ZVS buck converter shows the capabilities to switch at much higher frequencies compared to the conventional hard switching buck converter. The converter was built using 100V eGaN FETs but the input voltage has been limited to 50V for this experiment. The converter was tested at two different frequencies for investigating the performance with a change in the inductor. The converter running at 2 MHz uses a 2.2uH inductor and the efficiency achieved is 75% at 12V, 9W output load. The low efficiency is mainly due the inductor losses. The frequency changed to 6 MHz and a 500nH air core inductor was used to form the converter. The efficiency achieved was 83%.

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